REMARKS

This is a response to the non-final Office Action dated September 7, 2004.

Regarding paragraph 1 of the Office Action and the objection to Fig. 2D, Applicant notes that, in the preliminary amendment filed with the application on November 5, 2003, the paragraph of the specification between page 8, line 24 and page 9, line 2 was amended to refer to "words 44a, 44b, 44c, 44d" (see page 6 of the preliminary amendment).

Regarding paragraph 2 of the Office Action, claim 11 has been amended to correct a typographical error.

Claims 1, 3, 4, 11, 13-15, 17-22 and 25-28 are amended. Claims 2 and 5-10 are cancelled. Claims 12, 16, 23 and 24 are unchanged. Claims 29-32 are new. See the deletion or repetition pattern of Fig. 2d, and pages 8-9, bridging sentence, of the specification.

Claims 1, 3, 4, 6 and 11-30 have been rejected under 35 U.S.C. §112, second paragraph. Without conceding to the propriety of the rejection, claims 1, 20, 27 and 28 have been amended to refer to a bit "deletion or repetition" pattern.

Regarding claims 1, 20, 27 and 28, and the selection of a bit deletion or repetition pattern that ensures that the deleted or repeated bits are not required to enable all bits from the digital input signal to be reconstructed, note that this limitation is explained, e.g., in connection with Figs. 2c and 2d and page 7, line 23 – page 9, line 10 of the specification. For example, as explained at page 8, lines 18-23, and referring to Fig. 2c, if every fourth bit is deleted or repeated when the block of data is read out, column by column, the result will be to delete or repeat four adjacent bits in the first and fifth rows, which is disadvantageous. In contrast, the deletion or

repetition pattern of Fig. 2d, where each column in the pattern or matrix is offset from the previous column, is advantageous because it avoids deleting or repeating adjacent bits (pages 8-9, bridging sentence). This achieves the claimed goal of enabling all bits from the digital input to be reconstructed without the deleted or repeated bits. Regarding the assertion that the claimed limitation is not tied to any structural limitation, Applicant respectfully notes that claim 1, for example, recites a transmitter including a rate matching circuit for adjusting the number of bits in a data block using a rate matching pattern, and means for selecting the rate matching pattern depending on the selected bit deletion or repetition pattern. Accordingly, the claimed limitation regarding the selection of the bit deletion or repetition pattern is clearly tied to a structural limitation (see, e.g., blocks 18 and 28, Fig. 1). Regarding the assertion that reciting a purpose for bit insertion or deletion in the negative is improper, note that negative limitations in claims are not improper (See, e.g., MPEP 2173.05(i), which states that "The current view of the courts is that there is nothing inherently ambiguous or uncertain about a negative limitation".)

Regarding claim 3, the rate matching pattern for each interleaved word is offset with respect to the rate matching pattern of the adjacent interleaved word or words. Fig. 2c clearly indicates an example of rate matching patterns, e.g., a pattern of 0's and 1's such as 100000100 and 010000010, that are offset as claimed. In this case, the bit position of the 1's is offset. See page 8, line 24 – page 9, line 2. The degree of offset is specified as being with respect to the adjacent interleaved word or words.

Regarding claim 14, this claim recites that "the rate matching pattern forms a matrix including change bits". Applicant respectfully submits that "change bits" are being introduced here as being part of the matrix. There is no term such as "the" or "said" before "change bits" indicating an antecedent reference. Accordingly, there is no lack of antecedent basis.

Claim 14 is rejected under 35 U.S.C. §112, second paragraph as being incomplete for omitting a cooperative relationship for "change bits". Applicant notes that claim 14 sets forth that the change bits are part of a matrix that is formed by a rate matching pattern. The rate matching pattern is referred to in claim 1 as something that is used by a rate matching circuit, which in turn is part of the claimed transmitter. Accordingly, it is respectfully submitted that there is a clear cooperative relationship between "change bits" and the structure of claim 1.

Regarding claim 15, and the reference to one of: (a) a fixed code rate, and (b) a predetermined number of rates for a variable data source, this claim does not recite that there is a fixed rate and a variable rate at the same time. Only one or the other is claimed, not both. Without conceding to the propriety of the rejection, the claim has been amended to provide further clarity.

Claim 15 is rejected under 35 U.S.C. §112, second paragraph as being incomplete for omitting a structural cooperative relationship between the coding circuit, fixed code rate, and a predetermined number of rates for a variable data source. Applicant notes that the "coding circuit" is a structural element, while the "fixed code rate" and "the predetermined number of rates for a variable data source" are characteristics, not structural components, of the "coding circuit". Accordingly, there can be no structural relationship between the "coding circuit" and its characterizing features.

Regarding claim 18, please see the comments above regarding claim 15.

Regarding claim 21, please see the comments above regarding claim 14.

Regarding claim 22, please see the comments above regarding claim 15.

Regarding claim 25, please see the comments above regarding claim 15.

In view of the above, the questioned claim language is believed to clearly meet the requirements of 35 U.S.C. §112, second paragraph. Withdrawal of the rejections is therefore respectfully requested.

Claims 1, 3, 4, 11 and 14-28 have been rejected under 35 USC 102(b) as being anticipated by Okumura et al. (Okumura). Okumura is concerned with a variable rate data transmission scheme that allows continuous transmission. To achieve this, a coded data sequence (output from the block "convolutional coder & interleaver", Fig. 1) is transformed into a QPSK symbol sequence with symbol rate R. A repetition code is then used to replicate the symbol sequence based on an integral rate index Q=Rm/R, where Rm is the maximum symbol rate (p.2026, col. 2, bottom). For example, Q=1, 2 or 4 (p.2027, col. 1, bottom). Thus, the symbol sequence rate can essentially be doubled or quadrupled. In contrast, Applicant's claim 1, for example, is concerned with adjusting the number of bits in a data block, which comprises a plurality of interleaved words, using a rate matching pattern that depends on an associated bit deletion or repetition pattern that is selected to ensure that deleted or repeated bits of the data block are not required to enable all bits from a digital input to be reconstructed. Thus, Applicant's invention is concerned with deleting or repeating bits in a data block. Okumura fails to disclose or suggest this feature since he is repeating the entire data symbol sequence that has been formed after coding of data blocks, e.g., using convolutional coding and interleaving, has occurred. Furthermore, Okumura is not concerned with using a rate matching pattern to achieve the goal of adjusting the number of bits in a data block. The repetition code of 1, -1 used by Okumura is not a rate matching pattern as claimed because it is used for replicating an entire symbol sequence, not for adjusting the number of bits in a data block.

Withdrawal of the rejection is therefore respectfully requested.

Applicant's dependent claims similarly are patentable over Okumura.

For example, regarding claim 3, the spreading code used by Okumura is not analogous to Applicant's rate matching pattern, where the rate matching pattern for each interleaved word in a data block is offset with respect to the rate matching pattern of an adjacent interleaved word or words. This can be seen in that the spreading code of Okumura, which is a CDMA spreading code, is applied to the data symbol sequence after the sequence is replicated (Okumura, Fig. 1). Thus, there is only one spreading code, not different rate matching patterns that are offset as claimed.

Regarding claim 14, which depends on claim 1, as discussed above in connection with claim 1, the repetition code 1, -1 of Okumura is simply a multiplier used for repeating the entire data symbol sequence, but is not a rate matching pattern for achieving the goal of adjusting the number of bits in a data block as claimed. Even if the code 1, -1 could be thought of as a repetition pattern as asserted by the Examiner, this still does not provide a disclosure or suggestion of a rate matching pattern that forms a matrix including change bits as claimed that indicate a change of corresponding bits of interleaved words within a data block, wherein each row of the matrix includes a maximum of one of the change bits.

The remaining dependent claims of claim 1 are similarly patentable over Okumura.

Independent claim 20, relating to a receiver that is an analog of the transmitter of claim 1, is patentable over Okumura for the same reasons the transmitter of claim 1 is patentable over Okumura.

Regarding independent claim 27, relating to a method for operating a transmitter, and claim 28, relating to a method of operating a receiver, which are analogs of claim 1 and 20,

respectively, these claims are patentable over Okumura for the same reasons claims 1 and 20 are patentable over Okumura.

The remaining dependent claims are similarly patentable over Okumura.

Withdrawal of the rejection is therefore respectfully requested.

Dependent claims 12 and 13 have been rejected under 35 USC 103(a) as being unpatentable over Okumura et al. (Okumura) in view of U.S. patent 5,729,526 to Yoshida. Applicant respectfully asserts that it would not be obvious to combine the teachings of Okumura and Yoshida as suggested since they are concerned with different technical problems. Namely, Okumura is concerned with providing a single variable rate transmission that allows continuous transmission, while Yoshida is concerned with providing, from an input data stream, two channels with different quality, such as a higher-quality main channel for an ATM cell, and a lower-quality sub-channel for an ATM header (col. 4, lines 20-24). Regarding the asserted motivation that the use of additional coding devices with a multiplexer for combining their outputs would have provided the opportunity for transmitting ATM compliant data, Applicant notes that the provision of the sub-channel by Yoshida is not needed to transmit ATM data – it is just a particular technique for increasing the transmission rate within a fixed bandwidth (col. 4, lines 36-40) when ATM compliant data is transmitted. Moreover, the references, taken alone or in combination still fail to disclose or suggest the coding devices as claimed by the Application, or combining outputs of such coding devices as claimed.

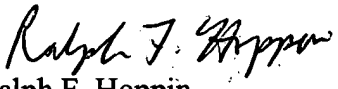
Withdrawal of the rejection is therefore respectfully requested.

Claims 1, 3, 4 and 11-28 have been rejected under the judicially created doctrine of double patenting in view of claims 1-19 of U.S. patent 6,671,851. Without conceding to the

propriety of the rejection, Applicant will consider filing a terminal disclaimer at such time as is needed for the application to proceed to issuance.

In view of the foregoing remarks herein, it is respectfully submitted that this application is in condition for allowance. Accordingly, it is respectfully requested that this application be allowed and a Notice of Allowance be issued. If the Examiner believes that a telephone conference with the Applicant's attorneys would be advantageous to the disposition of this case, the Examiner is requested to telephone the undersigned.

Respectfully submitted,



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